

FIG. 1

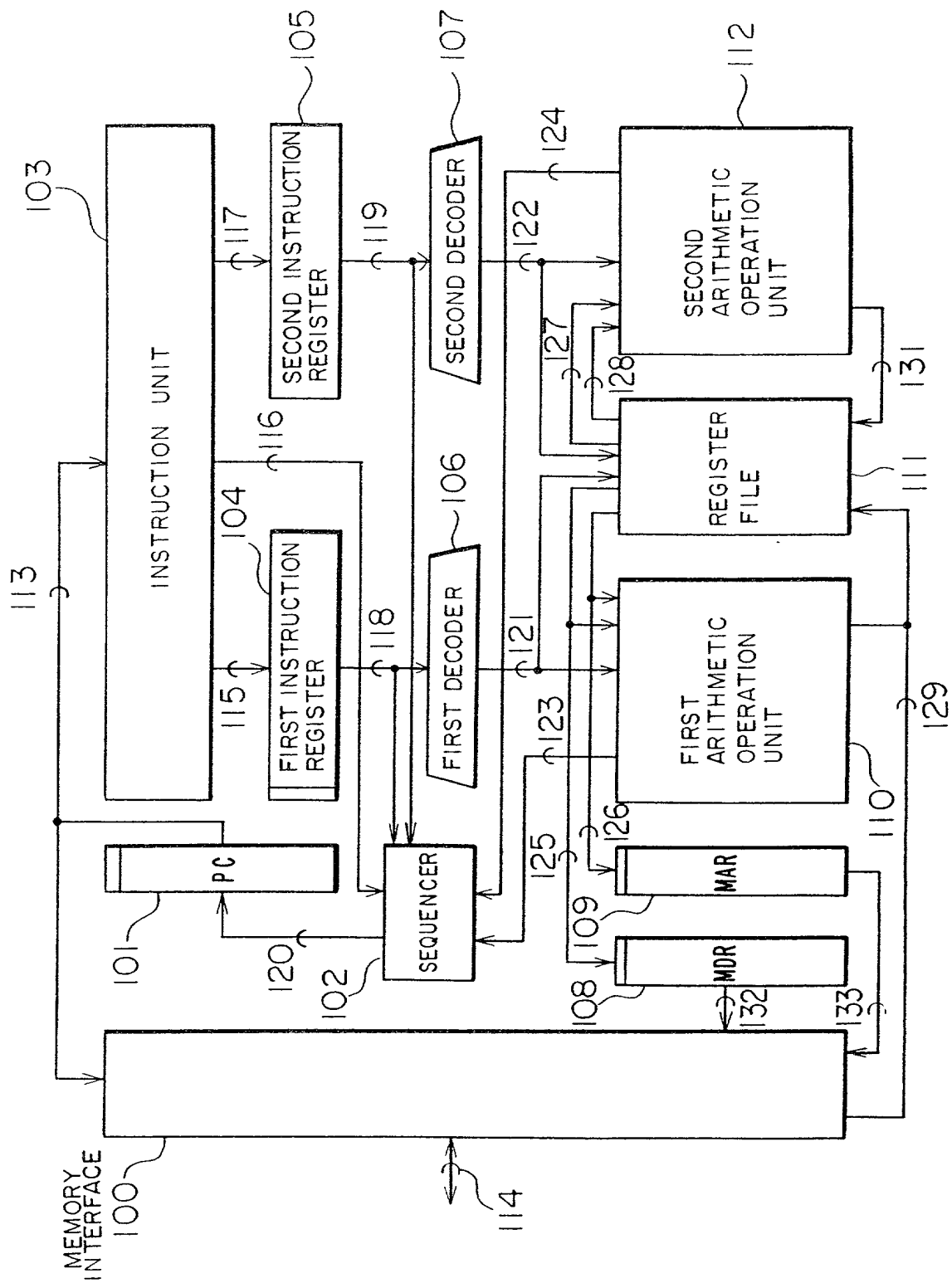


FIG. 2
PRIOR ART

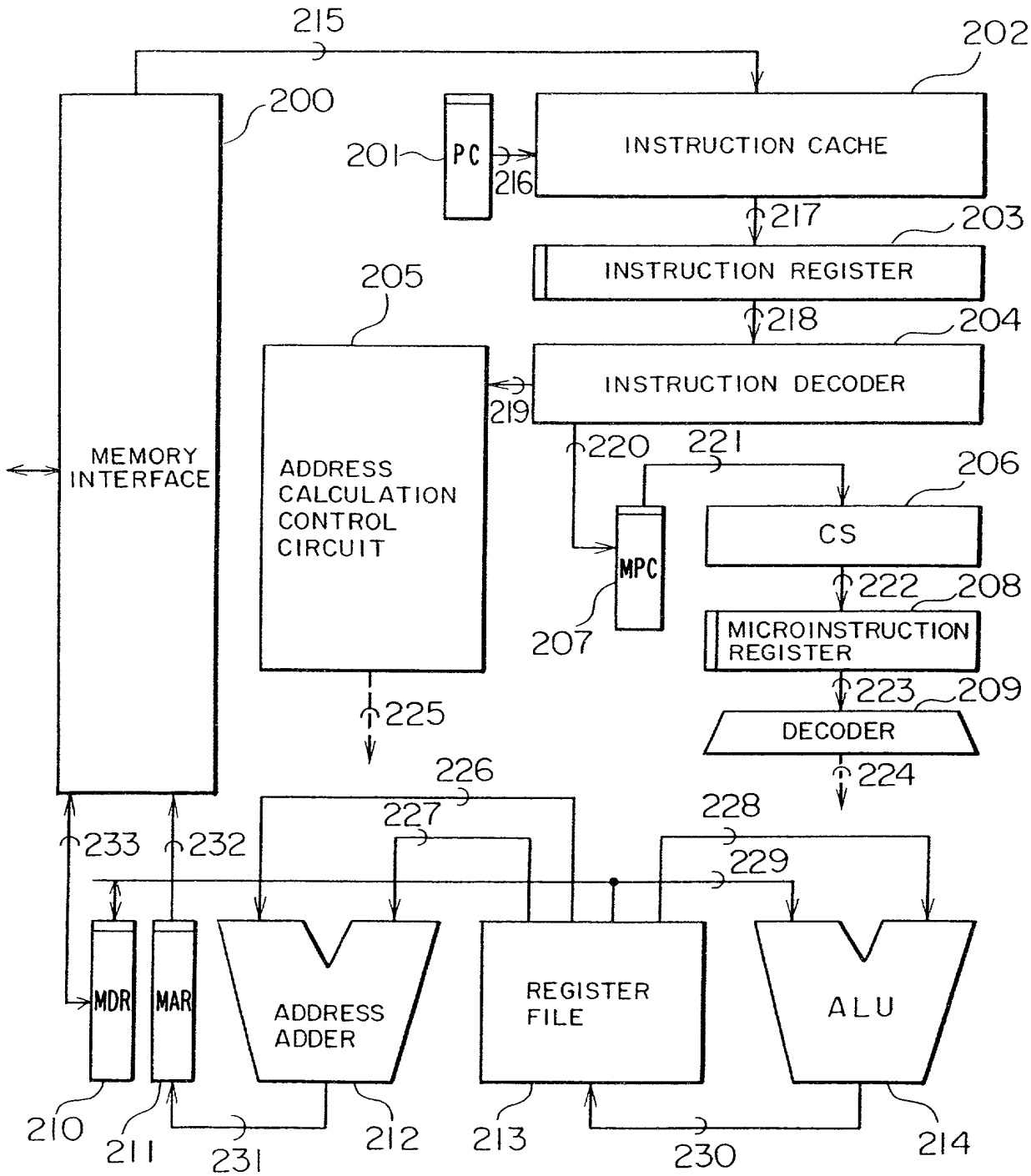


FIG. 3
PRIOR ART

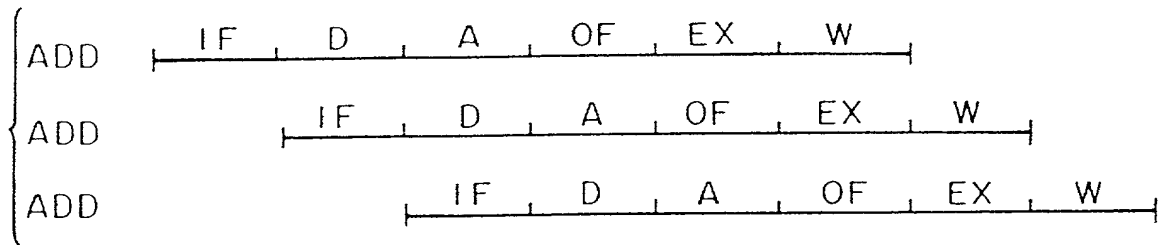


FIG. 4
PRIOR ART

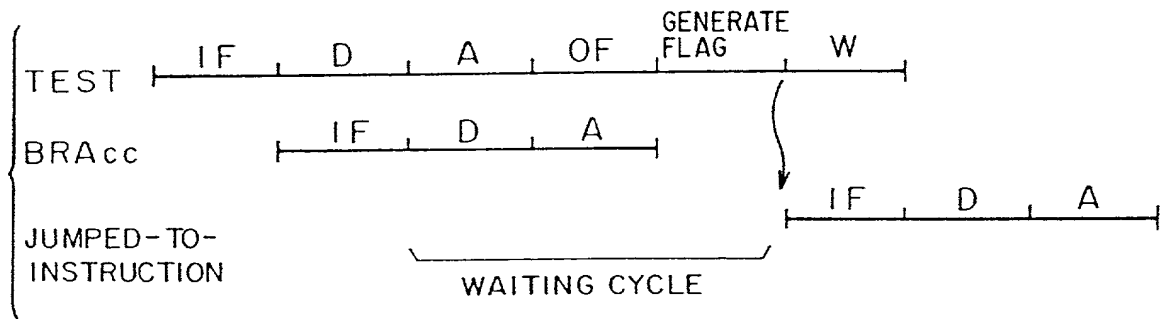


FIG. 5
PRIOR ART

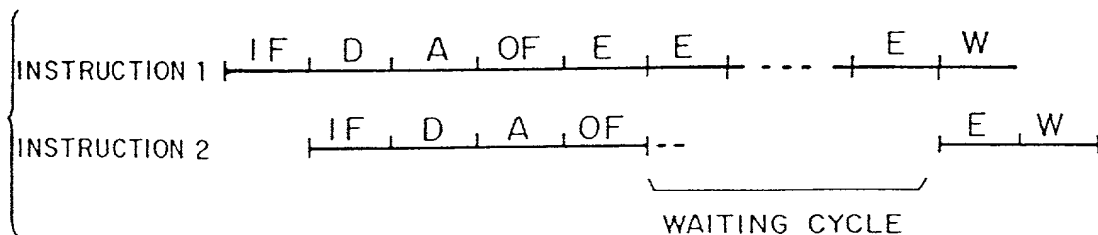


FIG. 6
PRIOR ART

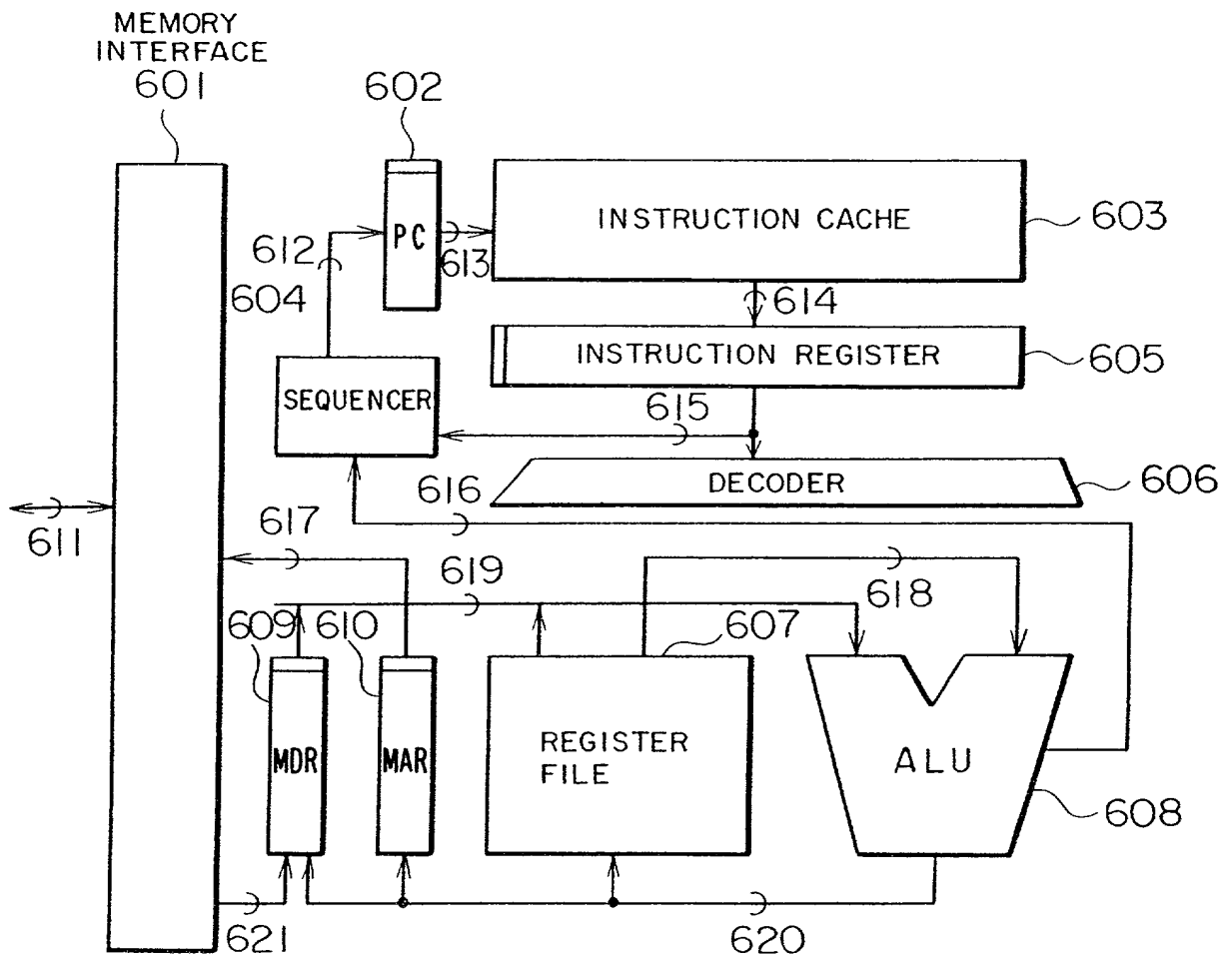


FIG. 7
PRIOR ART

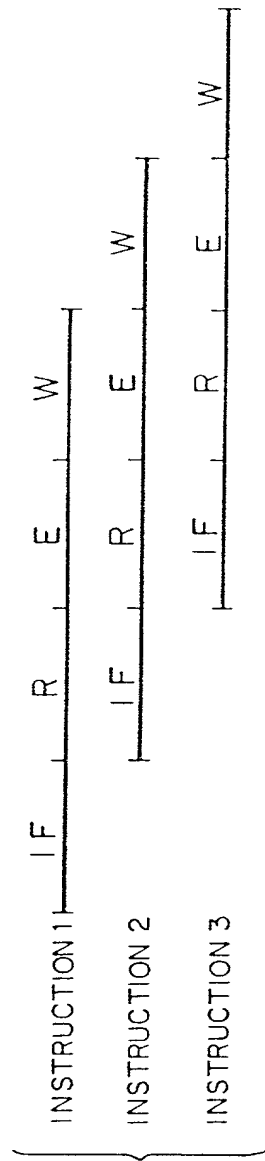


FIG. 8
PRIOR ART

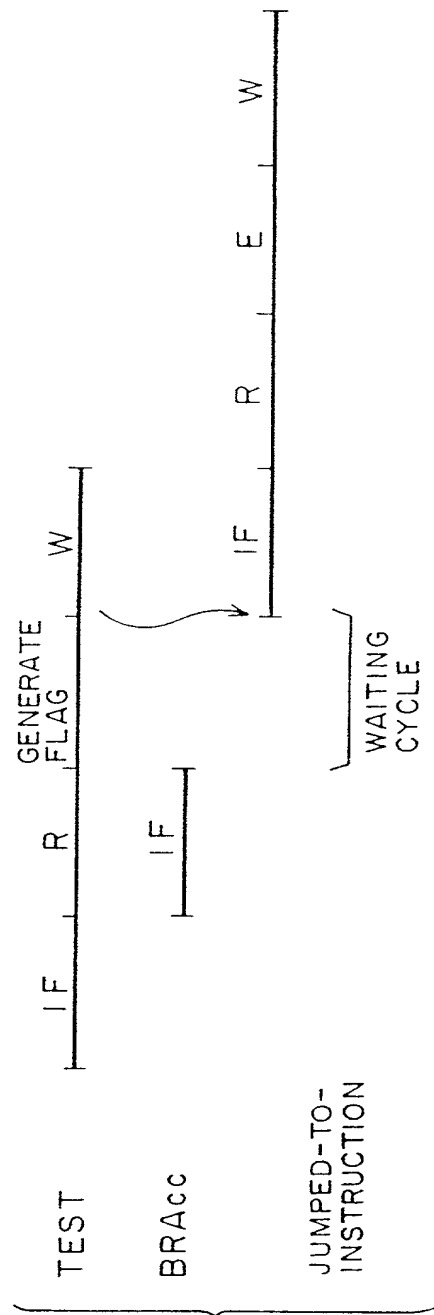
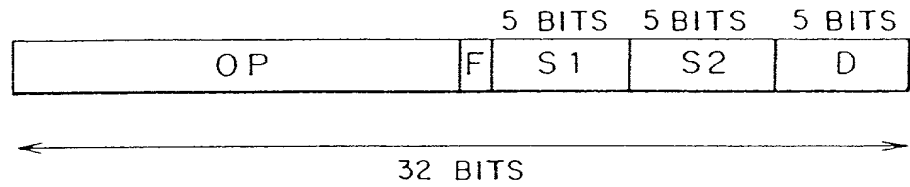


FIG. 9

TYPES	MNEMONIC	OPERATION
BASIC INSTRUCTION	ADD R(S1), R(S2), R(D)	$R(S1) + R(S2) \rightarrow R(D)$
	SUB //	$R(S1) - R(S2) \rightarrow R(D)$
	AND //	STORE LOGICAL PRODUCT OF EACH BITS OF R(S1), R(S2) IN R(D)
	OR //	STORE LOGICAL SUM OF EACH BITS OF R(S1), R(S2) IN R(D)
	EOR //	STORE EXCLUSIVE OR OF EACH BITS OF R(S1), R(S2) IN R(D)
	NOT R(S1), R(D)	STORE LOGICAL NOT OF EACH BIT OF R(S1) IN R(D)
	SFT R(S1), R(S2), R(D)	SHIFT R(S1) BY BIT NUMBER INDICATED BY R(S2) AND STORE IN R(D)
	NOP	DO NOTHING
BRANCH INSTRUCTION	BRA d	$PC + d \rightarrow PC$
	BRAcc d	
	CALL d	$PC \rightarrow R(0), PC + d \rightarrow PC$
	RTN d	$R(0) \rightarrow PC$
LOAD STORE INSTRUCTION	STOR R(S1), R(S2)	WRITE R(S1) IN MEMORY POINTED BY R(S2)
	LOAD R(S1), R(D)	WRITE DATA OF MEMORY POINTED BY R(S1) IN R(D)

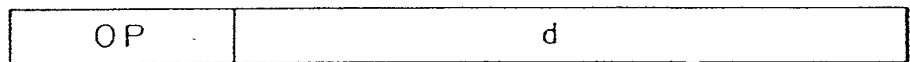
FIG. 10

1. BASIC INSTRUCTION

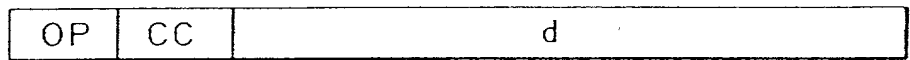


2. BRANCH INSTRUCTION

BRA, CALL
RTN



BRAcc



3. LOAD STORE INSTRUCTION



FIG. 11

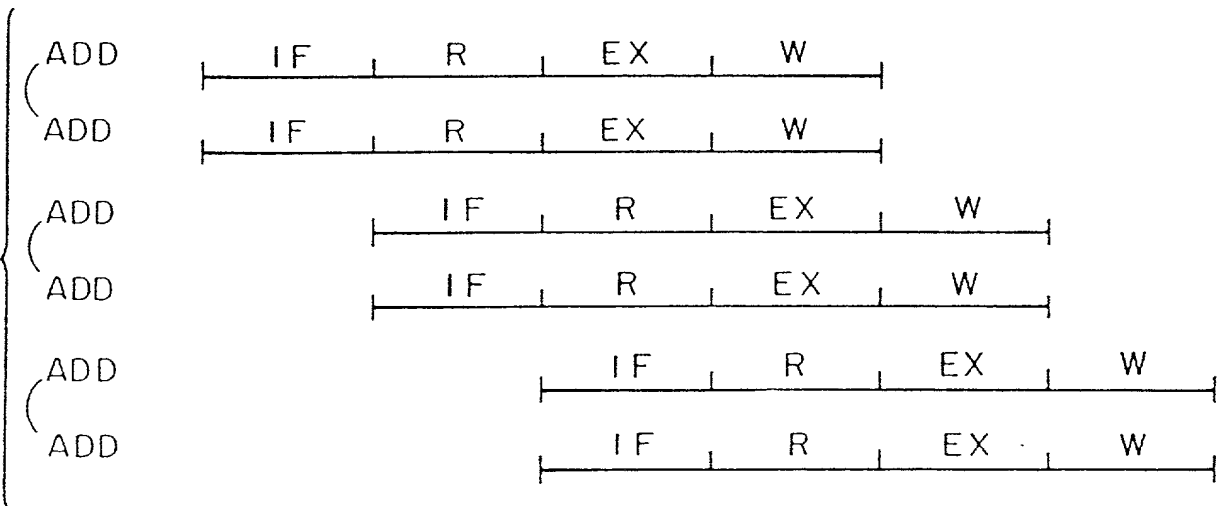


FIG. 12

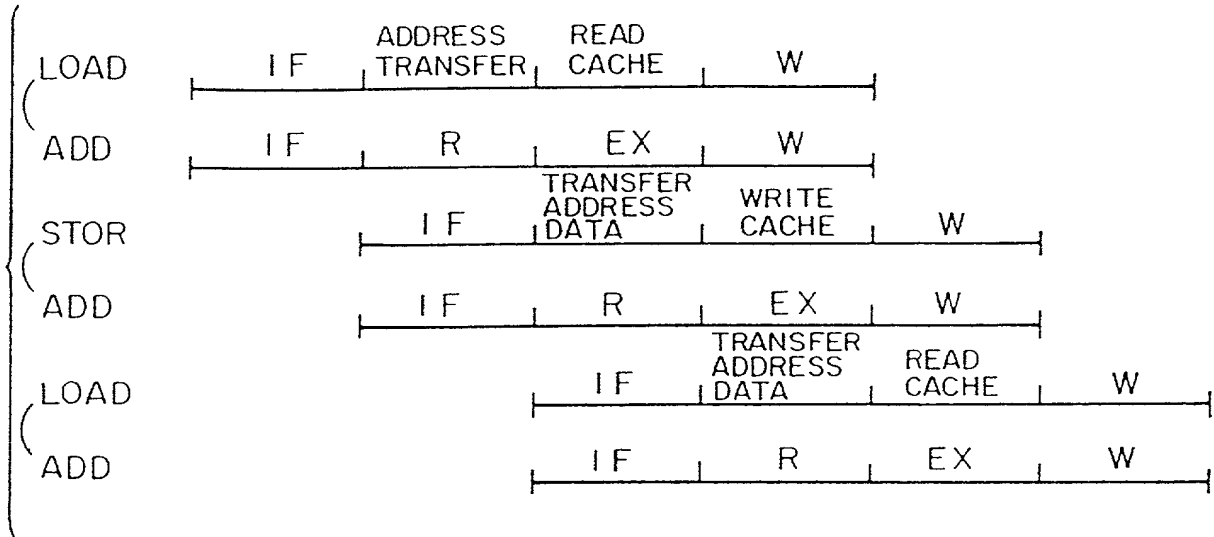


FIG. 13

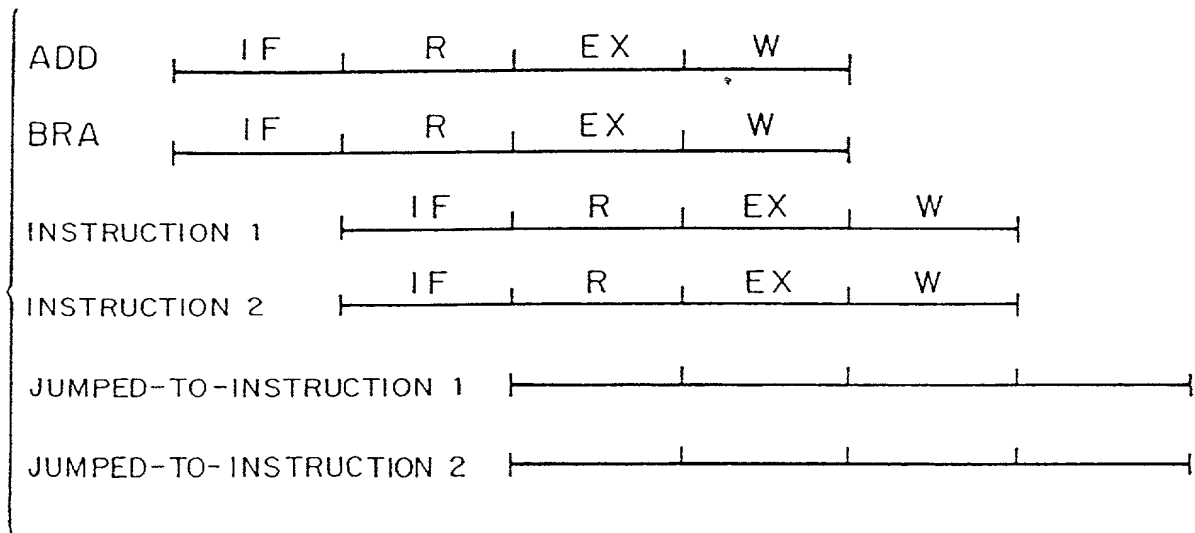


FIG. 14

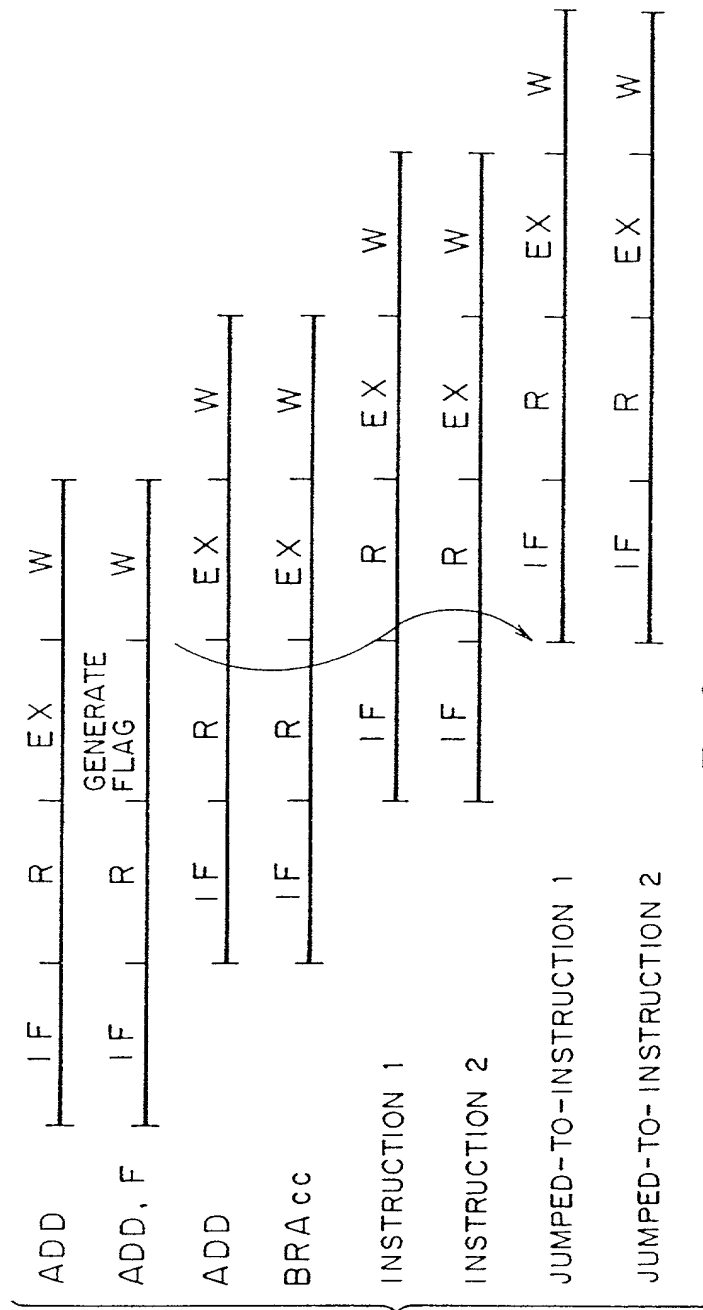


FIG. 15 PRIOR ART

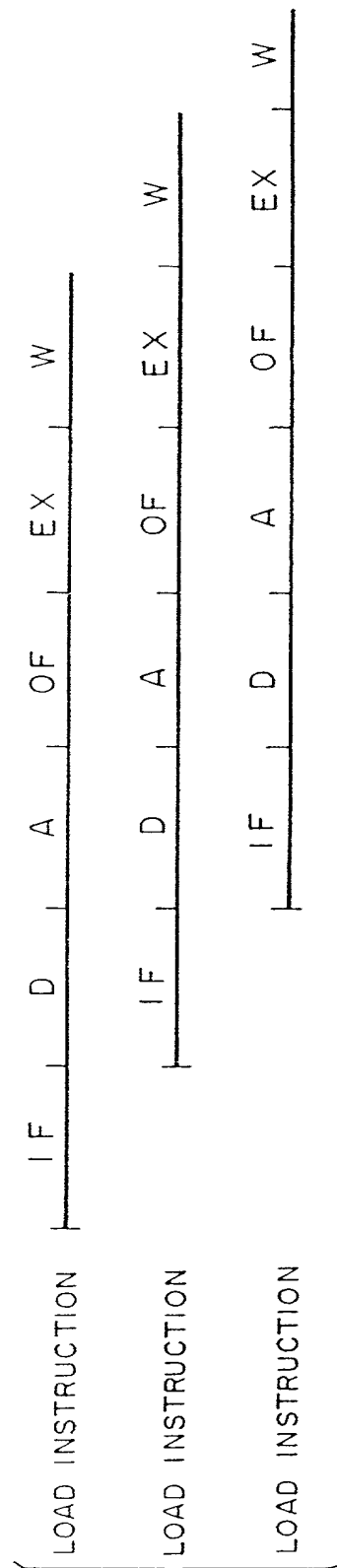


FIG. 16

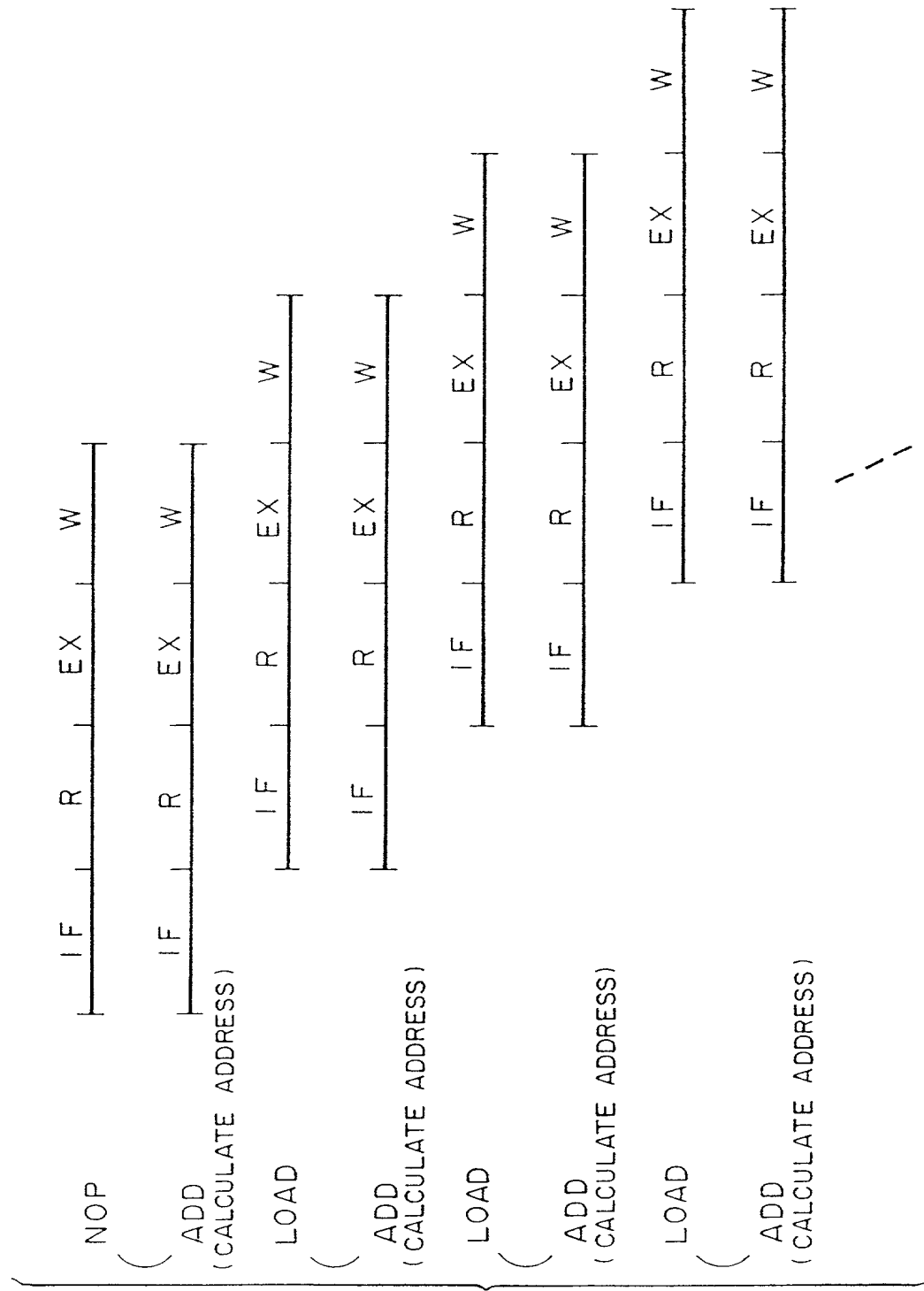


FIG. 17.
PRIOR ART

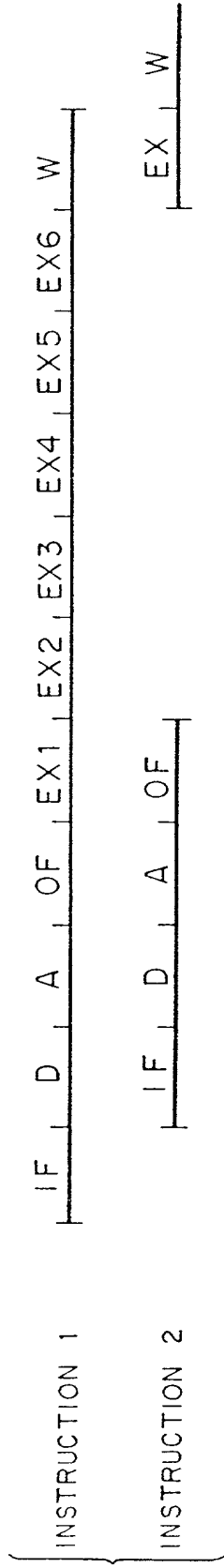


FIG. 18

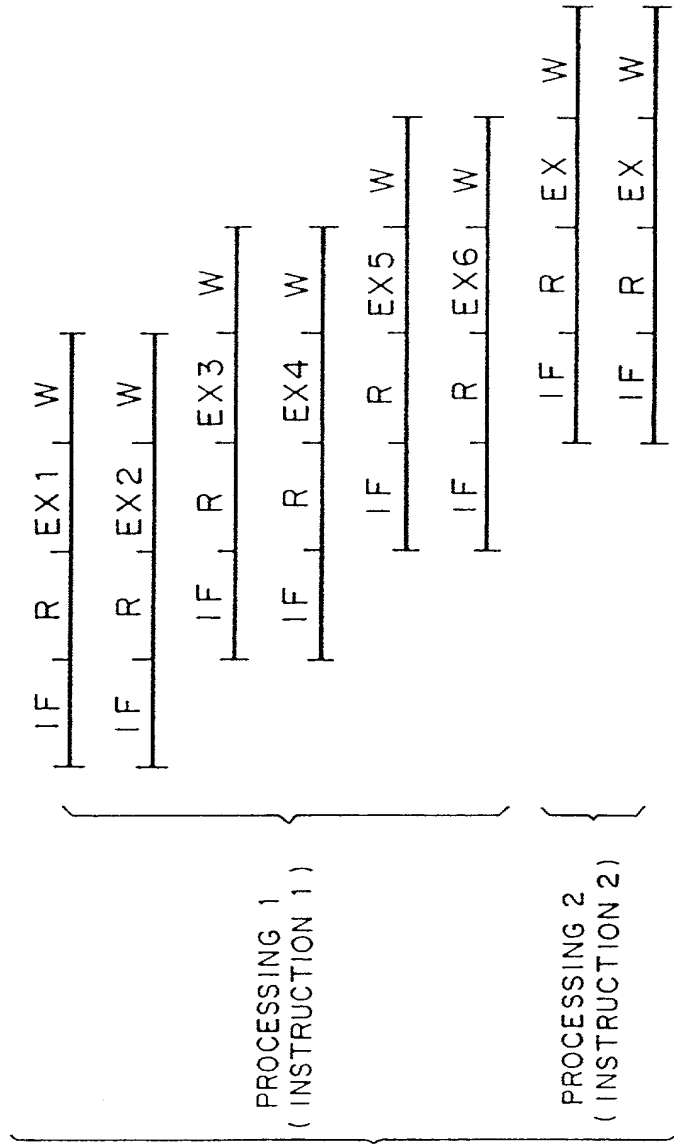


FIG. 19

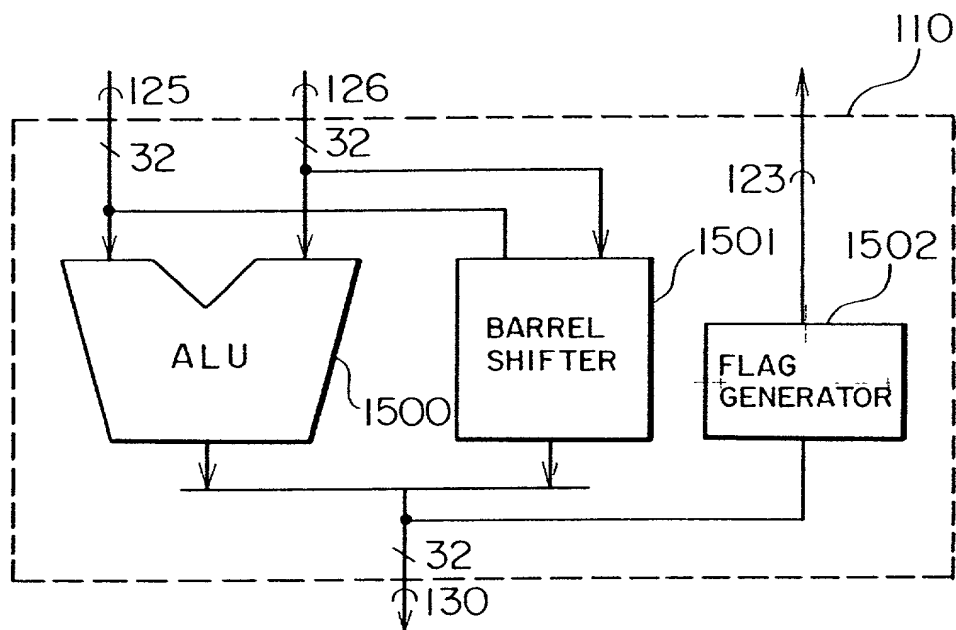


FIG. 20

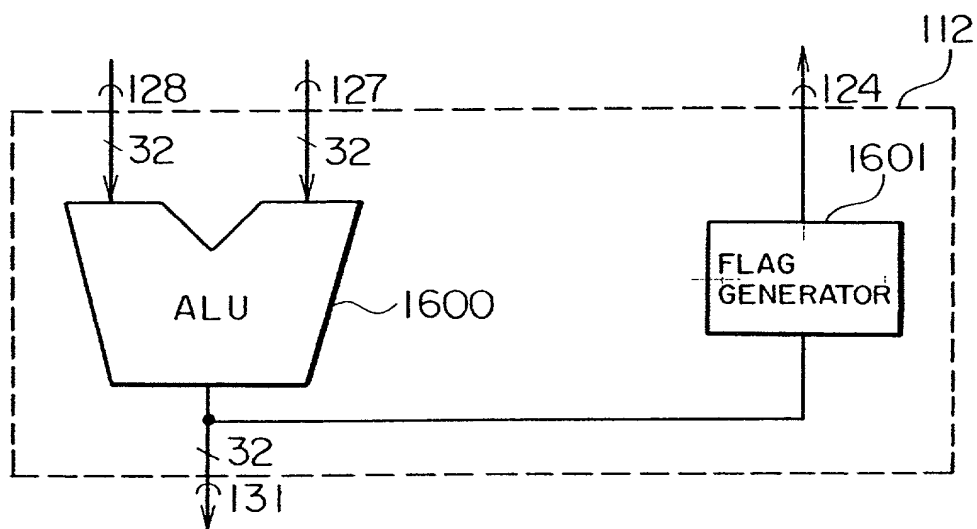


FIG. 22

ADDRESS	FIRST INSTRUCTION			SECOND INSTRUCTION		
0	SFT	R(1),	R(2),	R(3)	ADD	R(4), R(5), R(6)
2	SFT	R(7),	R(8),	R(9)	SFT	R(10), R(11), R(12)
4	ADD	R(14),	R(15),	R(16)	ADD	R(17), R(18), R(19)
			↓			
PC						
0	SFT	R(1),	R(2),	R(3)	ADD	R(4), R(5), R(6)
2	SFT	R(7),	R(8),	R(9)	NOP	
3	SFT	R(10),	R(11),	R(12)	NOP	
4	ADD	R(14),	R(15),	R(16)	ADD	R(17), R(18), R(19)

FIG. 23

ADDRESS						
0	SFT	R(1),	R(2),	R(3)	ADD	R(4), R(5), R(6)
2	SFT	R(7),	R(8),	R(9)	NOP	
4	SFT	R(10),	R(11),	R(12)	NOP	
6	ADD	R(14),	R(15),	R(16)	ADD	R(17), R(18), R(19)

FIG. 24

ADDRESS	FIRST INSTRUCTION	SECOND INSTRUCTION
0	ADD R(1), R(2), R(3)	ADD R(4), R(5), R(6)
2	LOAD R(3), R(10)	LOAD R(6), R(11)
4	ADD R(5), R(2), R(3)	ADD R(4), R(1), R(6)
↓		
PC	FIRST INSTRUCTION	SECOND INSTRUCTION
0	ADD R(1), R(2), R(3)	ADD R(4), R(5), R(6)
2	LOAD R(3), R(10)	NOP
3	LOAD R(6), R(11)	NOP
4	ADD R(5), R(2), R(3)	ADD R(4), R(1), R(6)

FIG. 25

ADDRESS	FIRST INSTRUCTION	SECOND INSTRUCTION
0	ADD R(1), R(2), R(3)	ADD R(4), R(5), R(6)
2	ADD R(1), R(5), R(8)	ADD R(8), R(9), R(10)
4	ADD R(12), R(13), R(14)	ADD R(15), R(16), R(17)
↓		
PC	FIRST INSTRUCTION	SECOND INSTRUCTION
0	ADD R(1), R(2), R(3)	ADD R(4), R(5), R(6)
2	ADD R(1), R(5), R(8)	NOP
3	ADD R(8), R(9), R(10)	NOP
4	ADD R(12), R(13), R(14)	ADD R(15), R(16), R(17)

FIG. 26

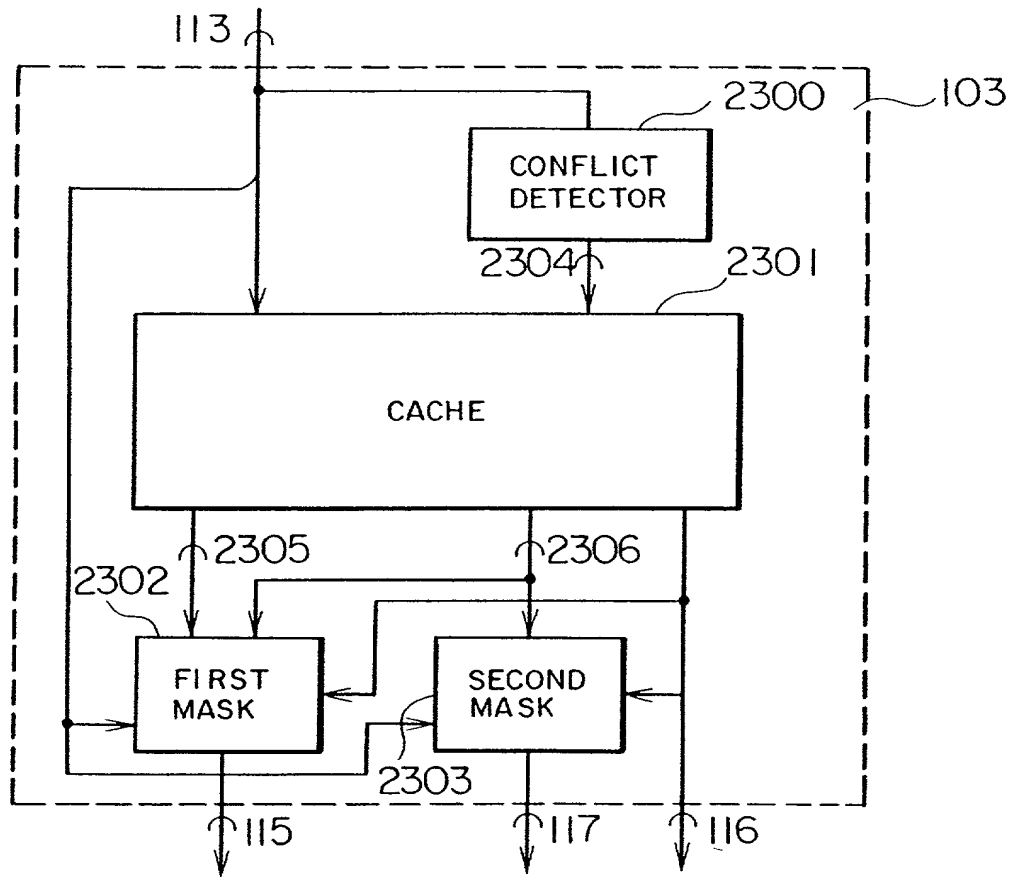


FIG. 27

CONFLICT BIT	LSB OF PC	FIRST INSTRUCTION SIGNAL 115	SECOND INSTRUCTION SIGNAL 117
0	0	FIRST INSTRUCTION	SECOND INSTRUCTION
0	1	NOP	SECOND INSTRUCTION
1	0	FIRST INSTRUCTION	NOP
1	1	SECOND INSTRUCTION	NOP

FIG. 28

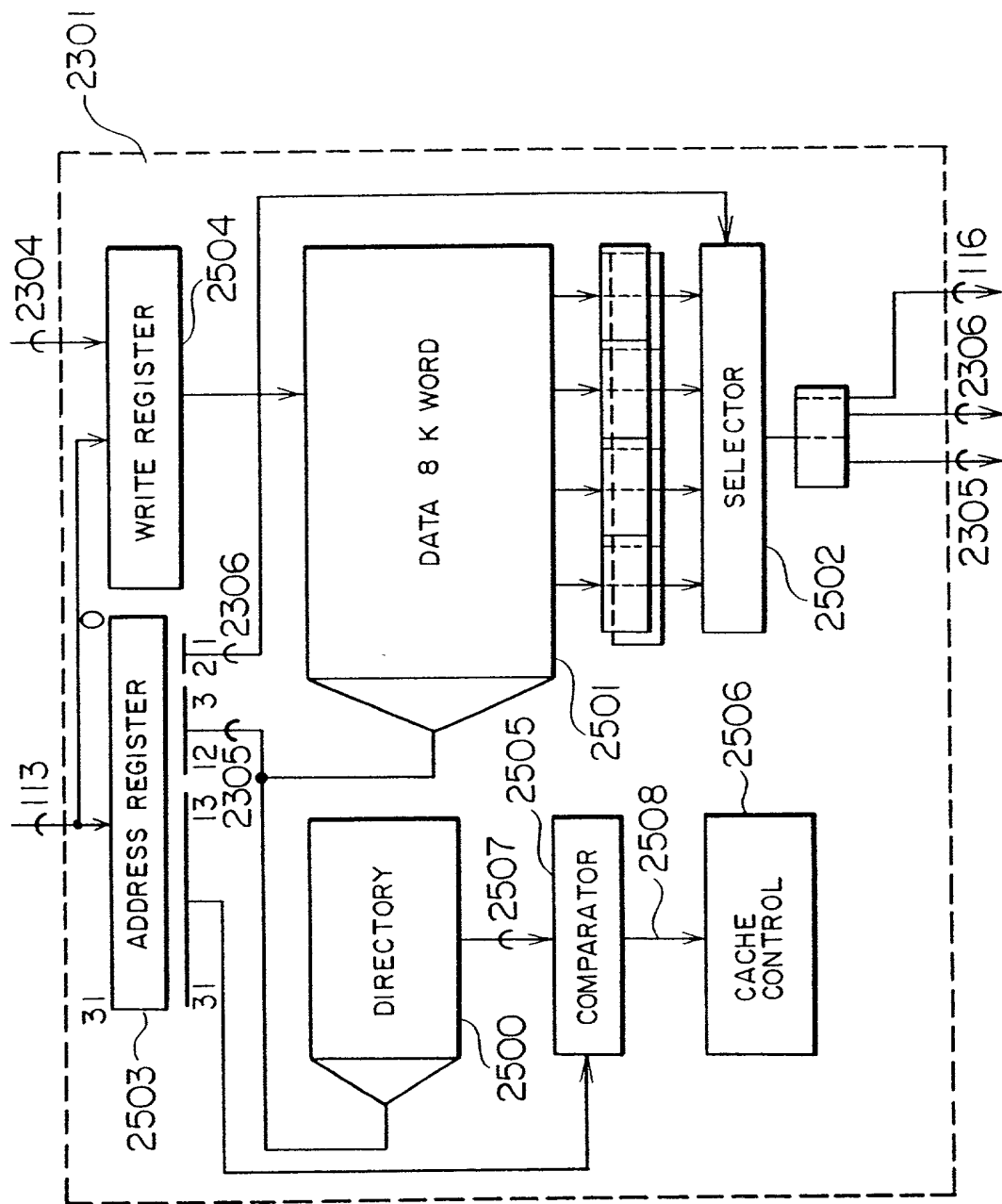


FIG. 29

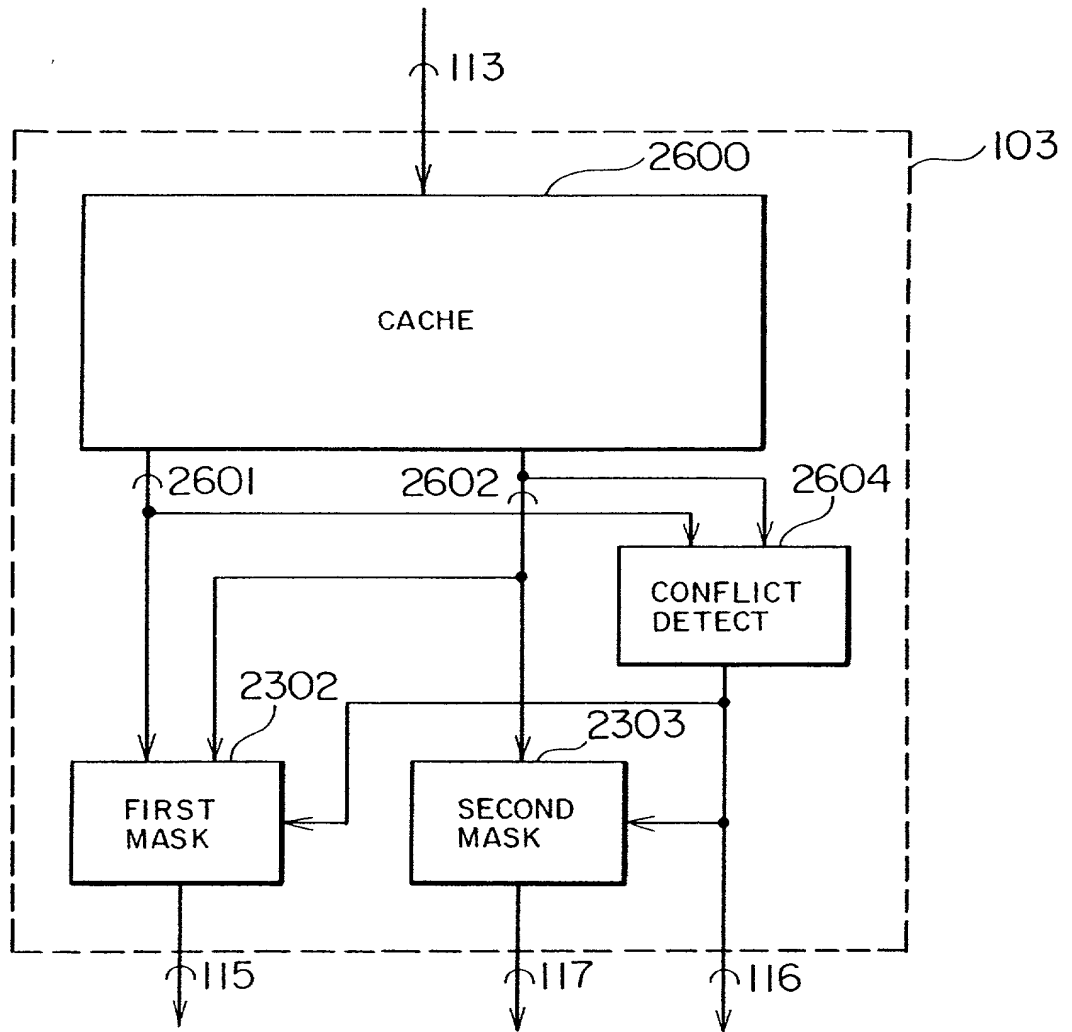


FIG. 30

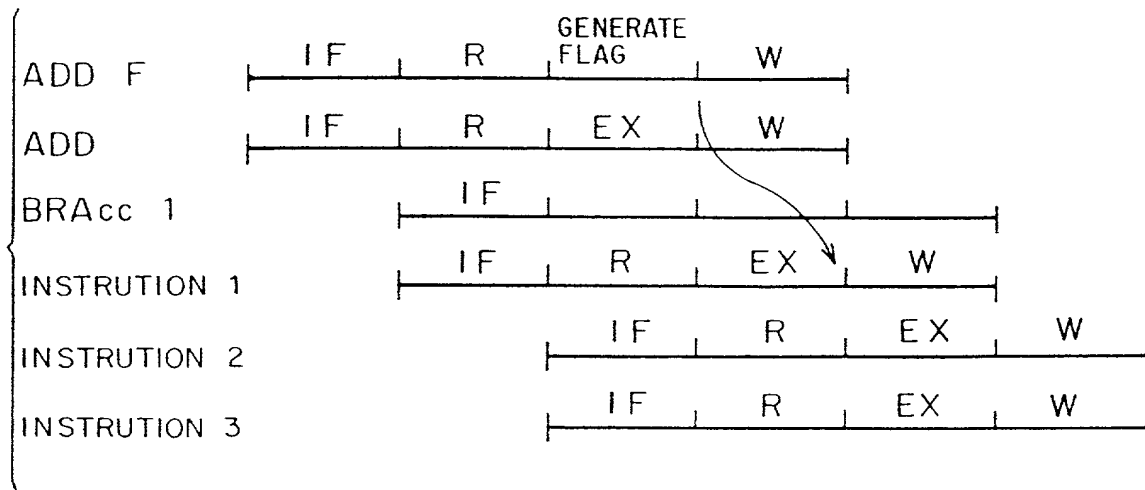


FIG. 31A
PRIOR ART

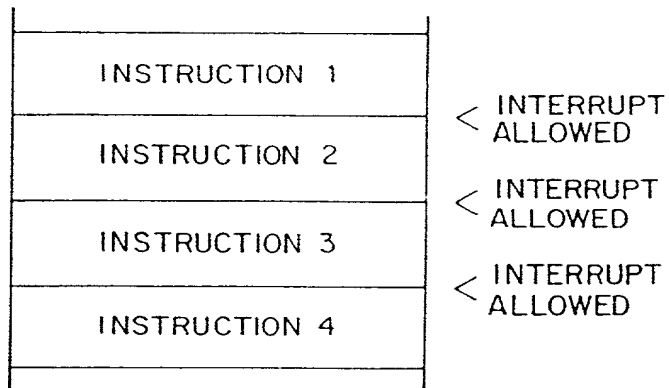


FIG. 31B

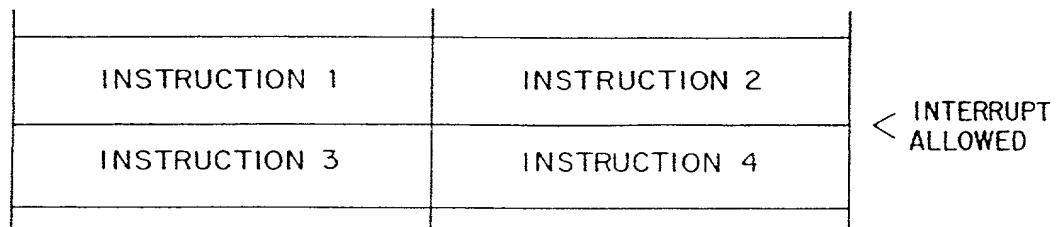


FIG. 32

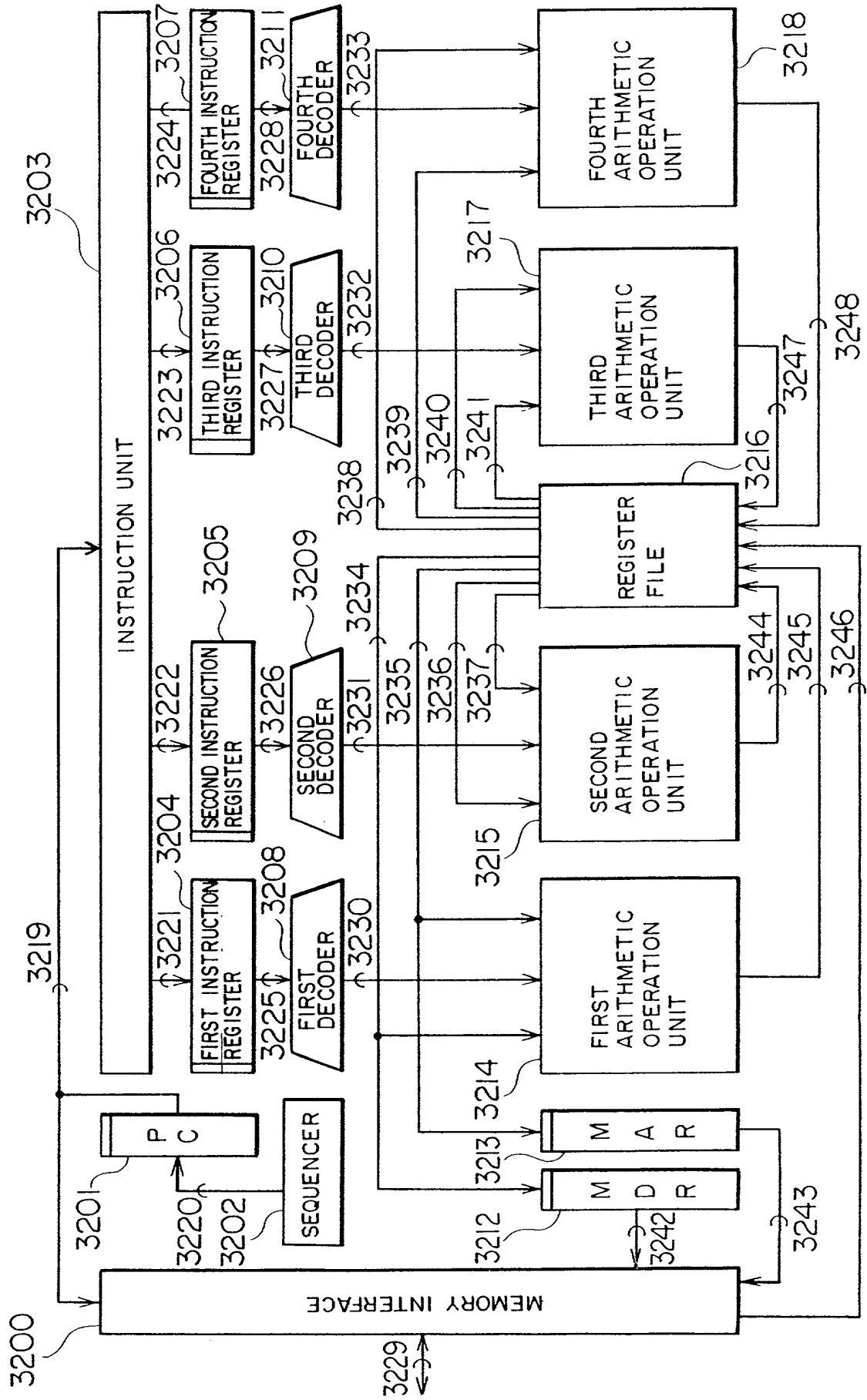


FIG. 33(a)

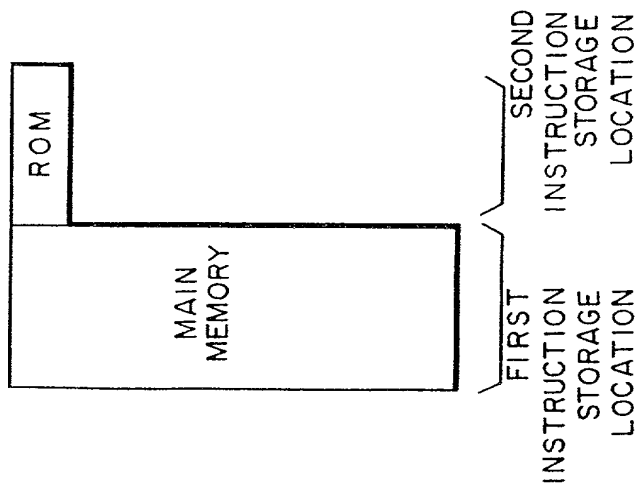


FIG. 33(b)

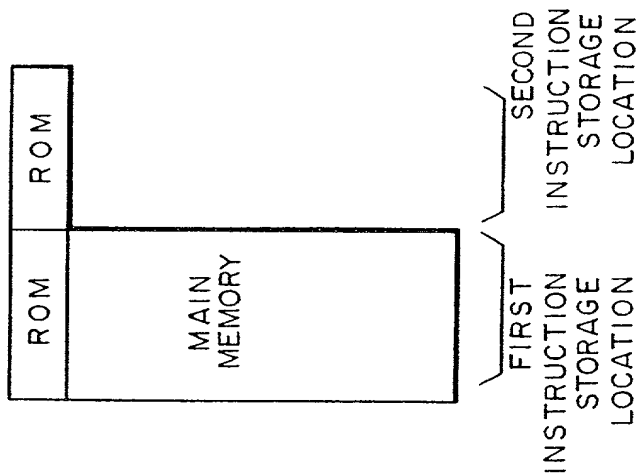
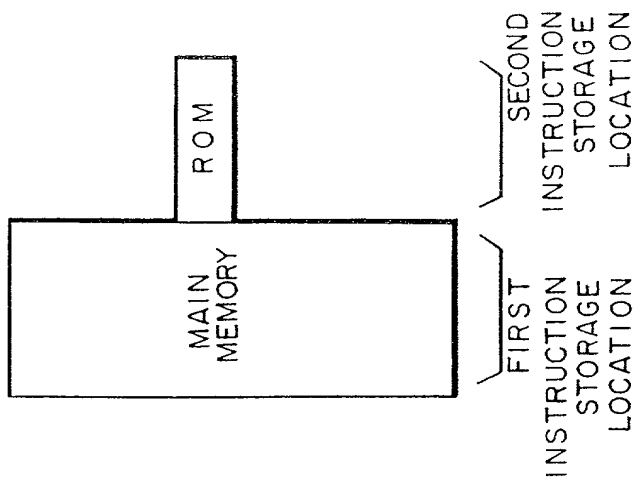


FIG. 33(c)



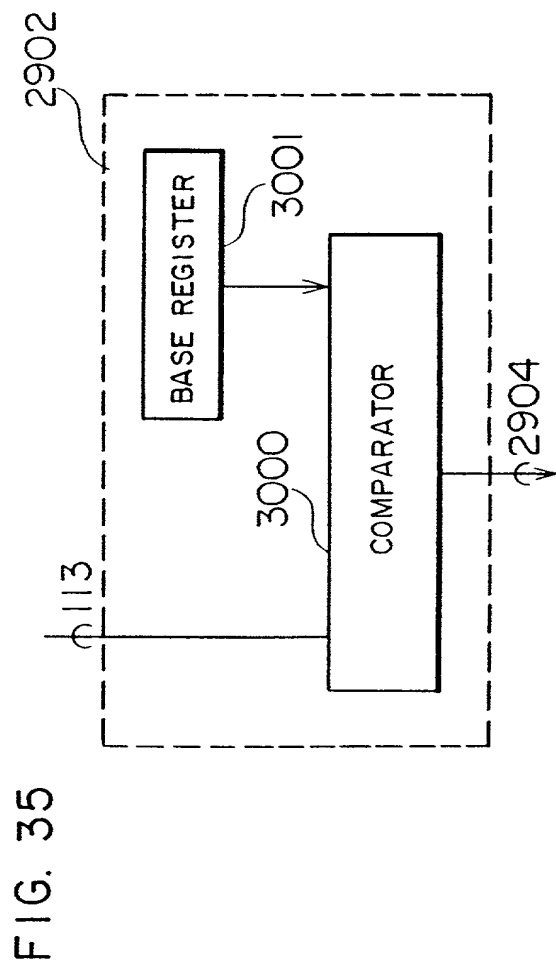
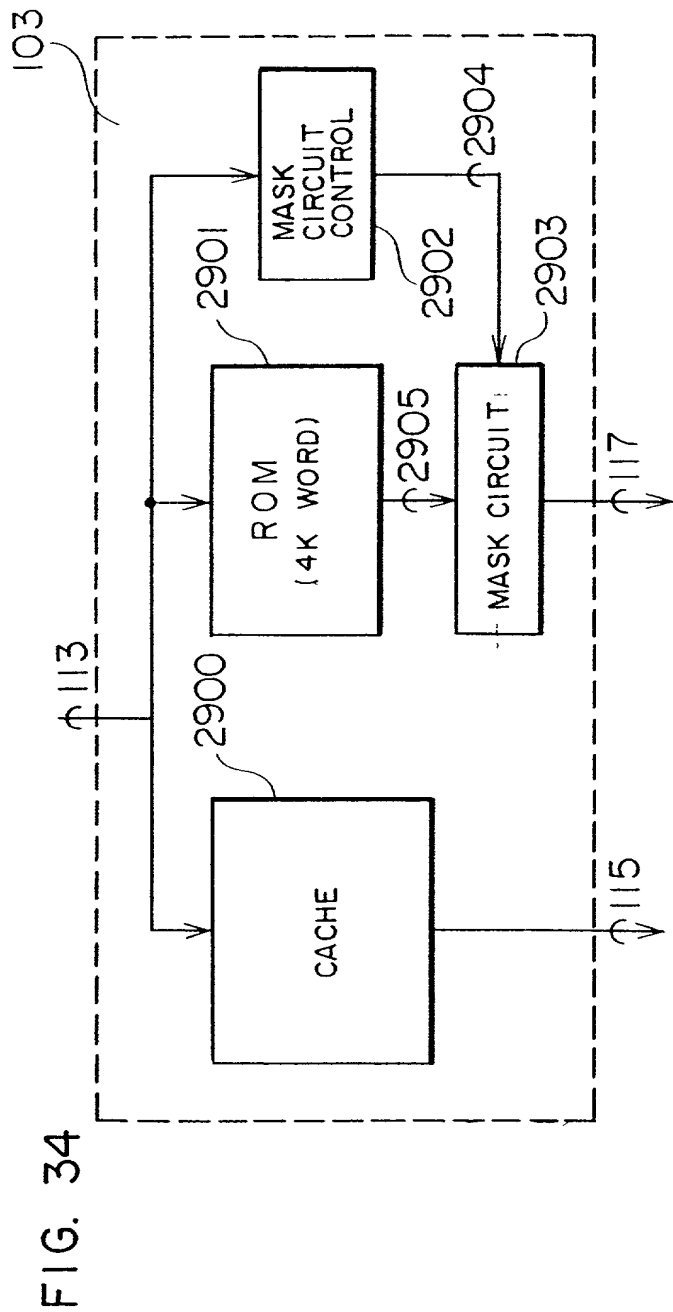


FIG. 36

